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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,279	12/28/2001	Hirobumi Yamaguchi	826.1780	2688

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EXAMINER

DAMIANO, ANNE L

ART UNIT	PAPER NUMBER
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2114

DATE MAILED: 06/24/2004

3

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/028,279

Applicant(s)

YAMAGUCHI ET AL.

Examiner

Anne L Damiano

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 28 December 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 13-15 is/are rejected.
- 7) ☒ Claim(s) 4-12 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

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## **DETAILED ACTION**

### ***Specification***

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### ***Allowable Subject Matter***

2. Claims 4-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### ***Claim Rejections - 35 USC § 112***

3. Regarding claims 14 and 15, the phrase "etc." renders the claim(s) indefinite because the claim(s) include(s) elements not actually disclosed (those encompassed by "or the like"), thereby rendering the scope of the claim(s) unascertainable. See MPEP § 2173.05(d). These claims are interpreted without the "etc."

### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

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A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3 and 13-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Cabezas et al. (US 2002/0095624).

As in claim 1, Cabezas discloses a pseudo I/O device (adapter and bus) for use in a pseudo I/O system that is connected to a device to be tested, and simulates an actual I/O system (A bus is an input/output device.), comprising:

A setting unit receiving a file where contents of an error of a pseudo target are defined and set, and setting the file as a setting file (firmware) (paragraph 35 and paragraph 36: lines 15-17); (The type of error to be injected to the PCI slot is stored in the firmware and must have been set at some point.)

A receiving unit receiving a command from the device to be tested (data pattern) (paragraph 31: lines 1-6);

A pseudo I/O unit (adapter and bus) processing the command received by said receiving unit according to set contents if the contents corresponding to the command are set when referencing the setting file (paragraph 35 and paragraph 36); and

Performing a normal reply process if the contents corresponding to the command are not set (paragraph 36: lines 5-15); and

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A transmitting unit returning data after being processed to the device to be tested (CPU tested) at a request source (paragraphs 35 and 36). (The system inputs error into a PCI slot according to the data stored in the firmware (a file) (paragraph: 35: lines 3-7). Data patterns (commands) are written to the adapter, which is controlled by the bus (paragraph 36: lines 5-7). If the setting file indicated that an error be injected into the bus, the pseudo I/O unit should return an error code (paragraph 35: lines 7-19). If the contents are not set, meaning no PCI error was inserted, a normal reply is returned which is a returning the data pattern (paragraph 36: lines 5-14).)

As in claim 2, Cabezas discloses the pseudo I/O device according to claim 1, wherein a file where information of an I/O device to be simulated is defined and set is set as the setting file (paragraph 9: lines 4-6 and figure 2: bus slots 1-4). (There are multiple bus slots that can be tested at a time, meaning that some form of indication as to which should be tested at a given time must be defined and set.)

As in claim 3, Cabezas discloses the pseudo I/O device according to claim 2, further comprising

A processing unit deleting predetermined set contents or restoring the set contents to normal set contents after performing a process according to the set contents if the predetermined contents are set when referencing the setting file, and automatically performing a normal reply process at a next time (paragraph 36).

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As in claim 13, Cabezas discloses a pseudo I/O method simulating an actual I/O device by making a connection to a device to be tested, comprising:

Receiving a file where error contents of a simulation target are defined and set, and setting the file as a setting file (firmware) (paragraph 35 and paragraph 36: lines 15-17); (The type of error to be injected to the PCI slot is stored in the firmware and must have been set and received at some point.);

Receiving a command from the device to be tested (data pattern) (paragraph 31: lines 1-6);

Performing a pseudo I/O process (adapter and bus) in which the received command is processed according to set contents if contents corresponding to the command are set when referencing the setting file (paragraph 35 and paragraph 36), and a normal reply process is performed if the contents corresponding to the command are not set (paragraph 36: lines 5-15); and

Returning the data after being processed to the device to be tested at a request source (paragraphs 35 and 36). (The system inputs error into a PCI slot according to the data stored in the firmware (a file) (paragraph: 35: lines 3-7). Data patterns (commands) are written to the adapter, which is controlled by the bus (paragraph 36: lines 5-7). If the setting file indicated that an error be injected into the bus, the pseudo I/O unit should return an error code (paragraph 35: lines 7-19). If the contents are not set, meaning no PCI error was inserted, a normal reply is returned which is a returning the data pattern (paragraph 36: lines 5-14).)

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As in claim 14, Cabezas discloses the pseudo I/O device according to claim 1, wherein the pseudo I/O device used to test operations of a test device of various types of devices (adapter and bus), an analyzer, a driver of an actual device, a driver installed on an OS, a RAID controller controlling a RAID device (paragraph 2).

As in claim 15, Cabezas discloses The pseudo I/O method according to claim 13, wherein the pseudo I/O method used to test operations of a test device of various types of devices (adapter and bus), an analyzer, a driver of an actual device, a driver installed on an OS, a RAID controller controlling a RAID device (paragraph 2).

### *Conclusion*

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See PTO-892.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anne L Damiano whose telephone number is (703) 305-8010. The examiner can normally be reached on M-F 9-6:30 first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ALD



**SCOTT BADERMAN**  
**PRIMARY EXAMINER**